REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-9, 11, 12 and 14-18 remain active in this application, Claims 1, 8, 11, 14, 15, 16, 17, and 18 having been amended and Claims 10 and 13 canceled by the present amendment.

In the outstanding Office Action the specification and drawings were objected to as including informalities requiring correction; Claim 10 was rejected under 35 USC §112, first paragraph, as failing to comply with the written description requirement; Claim 11 was rejected under 35 USC §112, first paragraph, as failing to comply with the written description requirement; Claim 16 was rejected under 35 USC §112, second paragraph, as being indefinite; Claims 1 and 2 were rejected under 35 USC §102(b) as being anticipated by Ker et al (U.S. 6,249,410, "Ker 1"); Claims 3-6 and 9 were rejected under 35 USC §103(a) as being unpatentable over Ker 1, in view of Ker et al (U.S. 5,959,820, "Ker 2"); Claims 7 and 8 were rejected under 35 USC §103(a) as being unpatentable over Ker 1 in view of Ker 2 and Bishop et al (U.S. 5,272,371); Claims 12-14 were rejected under 35 USC §103(a) as being unpatentable over Ker 1 in view of Ker 2 and Metz et al (U.S. 5,400,202); Claim 15 was rejected under 35 USC §103(a) as being unpatentable over Ker 1 in view of Ker 2 and Metz et al and further in view of Court Decision *St. Regis Paper Co. v. Bemis Co.*, 193 USPQ 8; Claims 16 and 17 were rejected under 35 USC §103(a) as being unpatentable over Ker 1 in view of Lee et al (U.S. 6,365,938); and Claim 18 was rejected under 35 USC §103(a) as being unpatentable over Ker 1 in view of Lee et al and Nguen (U.S. 5,682,049).

In response to the objection to the drawings, Claim 8 has been amended to correct the recitation of the collector and the emitter to the first and second pads, respectively, consistent

with the original drawings. Accordingly, it is respectfully submitted that the objection to the drawings has been overcome.

In view of the cancellation of Claim 10, the issues raised with respect to Claim 10 are moot.

In response to the rejection of Claim 16 under 35 USC §112, second paragraph, as being indefinite, Claim 16 has been amended to clarify the claimed subject matter. Accordingly, the rejection of Claim 16 under 35 USC §112, second paragraph, is believed to have been overcome. If the Examiner disagrees, the Examiner is invited to telephone the undersigned who will be happy to work with the Examiner in a joint effort to derive mutually satisfactory claim language.

In response to the rejection of Claim 11 under 35 U.S.C. 112, first paragraph, Claim 11 has been amended to better conform to Applicants' FIG. 12 disclosure. To that end, the reference to "source" has been changed to --one end of the current path--, and the reference to "drain" has been changed to --another end of the current path--. By way of explanation, the circuit shown in FIG. 12 differs from the circuit shown in FIG. 10 in that bipolar transistor 86 is replaced with thyristor 90. The thyristor 90 is not driven directly by the switch circuit 65; it is driven through the use of the trigger circuit 91 having resistor element 99. If the thyristor 90 is driven directly by the switch circuit 65, it cannot be turned off.

The circuit shown in FIG. 12 employs the trigger circuit 91 having resistor element 99, instead of providing a path used for discharging the base of the thyristor 90. The circuit shown in FIG. 12 is driven by use of the trigger circuit 91 having resistor element 99. With this structure, the thyristor 90 can be turned on or off, and a reliable operation is ensured.

In particular, the potential applied to the third pad 53 becomes equal to the potential (i.e., potential Vss) applied to the second pad 52, due to resistor R, when a high ESD voltage is generated between the first pad 51 and the second pad 52. As a result, transistor N1 is

turned off, transistor P1 is turned on, and transistor N2 is turned on. The clamp circuit 55 can therefore be reliably activated.

With respect to original claim 11, the outstanding Official Action correctly notes that transistor N2 is turned off if the source corresponds to the upper terminal and the drain corresponds to the bottom terminal. Regretfully, in original claim 11, the "drain" is incorrectly described as "source", and the "source" is incorrectly described as "drain." This can be understood if the current flowing direction is looked at with respect to the circuit shown in FIG. 12. However, the original specification does not explicitly describe the current flowing direction that would support the correction. Therefore, Applicants hereby amend Claim 11 so as to be consistent with the support provided by FIG. 12. In view of the amendments to Claim 11, the outstanding rejection of Claim 11 is believed to have been overcome.

In the evaluation of Applicants' invention, it is pointed out that the control circuit according to the present invention applies a desired potential to the third pad (i.e., pad 53, FIG. 6) in accordance whether the semiconductor chip has been incorporated into the end product, thereby to render the clamp circuit conducting or non-conducting. On the other hand, the ESD detection means (i.e., element 345, FIG. 12) taught by Ker 1 automatically detects generation of an ESD charge and supplies a signal to the charge dissipation means (i.e., element 345, FIG. 12). Ker 1 does not suggest, however, that the charge dissipation means may be rendered conducting or non-conducting.

The ESD protection circuit according to the present invention need not have an ESD detection means. Capacitors and resistors that may constitute an ESD detection means are unnecessary. This decreases the surface area of the ESD protection circuit and, hence, the manufacturing cost of the ESD protection circuit according to the present invention.

Applicants respectfully submit that Ker 1 does not suggest the configuration of the present invention and differs in advantages that would result from the configuration. It is therefore respectfully submitted that the pending claims are clearly patentable over Ker 1.

Turning now to a consideration of the Metz et al patent, it is first noted that the outstanding Official Action equates the claimed third pad (i.e., pad 53, FIG. 6) to the Metz et al Vdd pad (i.e., the leftmost Vdd pad, FIG. 4a). However, it is respectfully submitted that the recited third pad differs from the Metz et al Vdd pad in the several respects. In particular, the recited third pad differs as to the potential to which it is set, i.e., whether it is set at a desired potential (the same potential as that applied to the second pad) or a floating potential, before the chip is incorporated into the end produce (that is, before power is supplied to the chip). As long as no power is supplied to the chip, the third pad remains open. Thus, the control circuit sets the potential of the third pad to the same value as that of the second pad.

In FIG. 12, for example, the potential applied to the third pad 53 becomes equal to the potential (i.e., Vss potential) applied to the second pad 52, due to resistor R, when a high ESD voltage is generated between the first pad 51 and the second pad 52. As a result, transistors N1, P1 and N2 are turned off, on and on, respectively. The clamp circuit 55 can therefore be reliably activated.

In the Metz et al. invention, the potential applied to the Vdd pad (i.e., the leftmost pad) is a floating one unless power is supplied to the chip. In other words, the Vdd pad is not always fixed at Vdd potential. In FIG. 4a, for example, the Vdd pad assumes floating state when a high ESD voltage is generated between the pad 15 and the ground. The potential applied to the pad 15 cannot let Vdd pad remain at 0 V, because an ESD charge is applied to the Vdd pad through the semiconductor substrate. The potential of the pad 15 may be a positive one, making it very possible that NMOS 42 is turned on. Once NMOS 42 is turned

on, the gate potential of NMOS 18 can no longer rise to a sufficient value. Inevitably, NMOS 18 cannot activate the SCR.

In contrast, according to Applicants' invention, the same potential as that of the second pad is applied to the third pad when no power is supplied to the chip. In the Metz et al. invention, the Vdd pad (leftmost pad) is floating when no power is supplied to the chip; any desired potential cannot be applied to the Vdd pad.

According to Applicants' invention, the third pad is not floating even before the chip is incorporated into the end product (no power is supplied to the chip). The clamp circuit can therefore be reliably activated. This helps to accomplish reliable ESD protection.

As can be understood from the above discussion, Metz et al. do not suggest the technique of performing reliable ESD protection before the chip is incorporated into the end product.

Furthermore, the Vdd pad shown in Metz et al. FIG. 4a is not an external terminal, as can be seen from FIG. 4a and the description related to FIG. 4a. The Vdd pad differs from pad 15; it seems to be a node that is connected to a Vdd potential in the chip. Metz et al. do not suggest the idea of performing reliable ESD protection before the chip is incorporated into the end product.

In summary, Metz et al. do not suggest the configuration of the present invention defined in the amended claims. Hence, the Metz et al. invention differs in advantages that would result from the configuration, and accordingly, it is respectfully submitted that the claimed invention patentably distinguishes over Kir 1 and Metz et al.. The remaining references are considered no more pertinent than Kir 1 and Metz et al. and the pending claims are likewise believed to be patentably distinguishing over the prior art of record.

Consequently, in view of the present amendment, and in light of the above discussion, no further issues are believed to be outstanding, and the present application is believed to be

in condition for allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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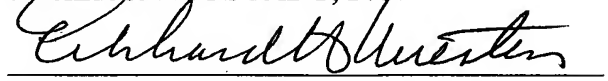

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